CLAIMS

1. An antifuse, comprising:

a bottom plate having a plurality of longitudinal members arranged substantially parallel to a first axis;

a dielectric layer formed on the bottom plate; and

a top plate having a plurality of longitudinal members arranged substantially parallel to a second axis, the top plate formed over the dielectric layer.

2. The antifuse of claim 1 wherein the first and second axes are substantially perpendicular.

3. The antifuse of claim 1 wherein each of the plurality of longitudinal members has a rectangular profile.

4. The antifuse of claim 1 wherein each of the plurality of longitudinal members comprises a vertically oriented plate having square corners along an upper edge on which the dielectric is formed.

5. The antifuse of claim 4 wherein each of the plurality of longitudinal members is formed from a tungsten material.

6. The antifuse of claim 1 wherein a plurality of edges are formed at intersections of the longitudinal members of the top and bottom plates.

7. A semiconductor structure, comprising:

a first plurality of semiconductor members extending longitudinally along a first axis;

a dielectric material formed over the first plurality of semiconductor members; and

a second plurality of semiconductor members extending longitudinally along a second axis and formed over the dielectric material.

8. The semiconductor structure of claim 7 wherein the first and second axes are substantially perpendicular.

9. The semiconductor structure of claim 7 wherein each of the first plurality of semiconductor members comprises at least one edge over which the dielectric material and the second plurality of semiconductor members are formed.

10. The semiconductor structure of claim 9 wherein each of the first plurality of semiconductor members comprises a vertically oriented plate having the at least one edge located at an upper portion of the respective semiconductor member.

11. The semiconductor structure of claim 7, further comprising:

a first interlayer;

a first plurality of slots formed in the first interlayer in which the first plurality of semiconductor members are formed;

a second interlayer formed over the first interlayer; and

a second plurality of slots formed in the second interlayer in which the second plurality of semiconductor members are formed.

12. An antifuse, comprising:

first and second pluralities of longitudinal members, the first and second pluralities of longitudinal members arranged substantially orthogonally with respect to one another, the second plurality overlying the first plurality; and

a dielectric interposed between the first and second pluralities of longitudinal members.

13. The antifuse of claim 12 wherein each of the longitudinal members of the first plurality have at least one edge on which the dielectric and second plurality of longitudinal members are formed.

14. The antifuse of claim 13 wherein each of the longitudinal members of the first plurality have a rectangular profile.

15. The antifuse of claim 12 wherein each of the longitudinal members comprise a vertically oriented rectangular plate.

16. The antifuse of claim 15, further comprising:

a first interlayer;

a first plurality of slots formed in the first interlayer in which the first plurality of longitudinal members are formed;

a second interlayer formed over the first interlayer; and

a second plurality of slots formed in the second interlayer in which the second plurality of longitudinal members are formed.

17. An antifuse, comprising:

a plurality of overlapping orthogonally arranged longitudinal members formed from semiconductor materials; and

a dielectric layer interposed between the overlapping orthogonally arranged longitudinal members coincident with the intersection thereof.

18. The antifuse of claim 17 wherein a first set of the plurality of longitudinal members have at least one edge on which the dielectric layer and a second set of the plurality of longitudinal members are formed.

19. The antifuse of claim 17, further comprising:

a first interlayer;

a first plurality of slots formed in the first interlayer in a first set of the plurality of longitudinal members are formed;

a second interlayer formed over the first interlayer; and

a second plurality of slots formed in the second interlayer in which a second set of the plurality of longitudinal members are formed.

20. A semiconductor structure formed on a substrate, comprising:

a first interlayer;

a first opening through the first interlayer exposing a portion of the substrate;

a local interconnect formed in the first opening and in contact with the substrate;

a first plurality of slots through the first interlayer;

a corresponding plurality of bottom plate members formed in a respective slot of the first plurality;

a dielectric layer formed on the plurality of bottom plate members;

a second interlayer formed over the first interlayer;

a second opening through the second interlayer exposing a portion of the local interconnect;

a contact plug formed in the second opening and in contact with the local interconnect;

a second plurality of slots through the second interlayer exposing portions of the dielectric layer, the second plurality of slots oriented substantially orthogonally with respect to the first plurality of slots; and

a corresponding plurality of top plate members formed in a respective slot of the second plurality.

21. The semiconductor structure of claim 20 wherein the local interconnect and the bottom plate members are formed from the same material.

22. The semiconductor structure of claim 21 wherein the local interconnect and the bottom plate are formed from a tungsten material.

23. The semiconductor structure of claim 20 wherein the contact plug and the top plate members are formed from the same material.

24. The semiconductor structure of claim 20 wherein the first opening and the first plurality of slots are formed concurrently.

25. The semiconductor structure of claim 20 wherein the second opening and the second plurality of slots are formed concurrently.

26. The semiconductor structure of claim 20 wherein each of the bottom plate members comprises a vertically oriented plate having at least one edge on which the dielectric layer is formed.

27. A method for forming an antifuse, comprising:

forming a first plurality of longitudinal members arranged substantially parallel to a first axis;

forming dielectric layer over at least a portion of the first plurality of longitudinal members; and

forming a second plurality of longitudinal members arranged substantially parallel to a second axis over the dielectric layer.

28. The method of claim 27 wherein the first plurality of longitudinal members are formed from a semiconductor material.

29. The method of claim 27 wherein the first and second axes are substantially perpendicular.

30. The method of claim 27 wherein forming the first plurality of longitudinal members is performed concurrently with formation of a local interconnect.

31. The method of claim 27 wherein forming the second plurality of longitudinal members is performed concurrently with formation of a contact plug.

32. A method for forming a semiconductor structure, comprising:

forming a plurality of overlapping orthogonally arranged members; and

forming a dielectric interposed between the overlapping members to electrically isolate the overlapping members from one another at intersections thereof.

33. The method of claim 32 wherein forming the overlapping orthogonally arranged members comprises:

forming a first interlayer;

forming a first plurality of openings in the first interlayer;

filling the first plurality of openings in the first interlayer with a first semiconductor material;

forming a second interlayer over the first interlayer;

forming a second plurality of openings in the second interlayer to expose the dielectric material;

filling the second plurality of openings in the second interlayer with second semiconductor material.

34. The method of claim 32, further comprising forming a local interconnect and forming a contact plug on the local interconnect, a first set of the plurality of overlapping members formed concurrently with the local interconnect and a second set of the plurality of overlapping members formed concurrently with the contact plug.

35. The method of claim 32 wherein forming the dielectric comprises forming the dielectric over a first set of the plurality of overlapping members, each member of the first set having at least one edge on which the dielectric is formed.